REMARKS/ARGUMENTS

After entry of this amendment, claims 1-12 and 46-53 will remain pending in this application. Claim 46 has been amended to correct a typographical oversight.

Claims 1-4, 7-10, 46-51, and 53 stand rejected under 35 U.S.C.§ 103(a) as being unpatentable over Nojima, United States patent number 6,246,634, in light of Sugita, United States patent number 5,276,842. Claims 5, 6, 11, 12, and 52 stand rejected under 35 U.S.C.§ 103(a) as being unpatentable over Nojima in light of Sugita, and further in view of Phelan, United States patent number 6,499,089. Reconsideration of these rejections and allowance of the pending claims is respectfully requested.

Claim 1

Claim 1 stands rejected under 35 U.S.C.§ 103(a) as being unpatentable over Nojima in light of Sugita. Specifically, the present office action states that it would be obvious to combine the arbiter in Sugita with the memory in Nojima, and that the resulting combination would anticipate claim 1. However, even if these references were combined, the combination does not show or suggest each and every element of this claim. Further, there is no motivation to combine these references as suggested.

For example, claim 1 recites "a programmable logic portion." The pending office action cites the Main Control Decoder Sequencer 60 in Figure 1 of Nojima as showing a programmable logic portion. (See pending office action, page 3, section 5.) But Nojima does not describe this circuit as being programmable, rather it is a fixed logic circuit configured to provide a specific logic function. (See Nojima, column 3, lines 11-33.) Thus, this circuit is not a programmable logic portion as is required by the claim.

Further, claim 1 recites "a processor." The pending office action cites the SRAM R/W Control circuit 54 of Nojima as providing this feature. (See pending office action, page 3, section 5.) While specific definitions of a processor may vary, applicants' submit that processors are understood by one skilled in the art to generally include at least one or more execution units, such as an arithmetic logic unit, multiply-accumulate unit, or fixed or floating point unit. (See

for example, Comprehensive Dictionary of Electrical Engineering, IEEE press, 1999.) But the SRAM R/W Control circuit 54 of Nojima is described as being a control circuit that provides read and write control signals for an SRAM memory bank. (See Nojima, column 3, lines 2-7.) Thus, Nojima does not describe this circuit as being a processor.

Also, there is no motivation to combine the arbiter of Sugita with the memory of Nojima. The arbitrating circuit of Sugita arbitrates access to a memory during an access conflict between its two ports. (See Sugita, column 2, lines 37-47.) But Nojima does not disclose a two port memory, rather, Figure 2 of Nojima shows a single port RAM having address and data multiplexers coupled to a single port. Thus, there are not two ports that can create an access conflict. That is, Nojima does not show a first port and a second port that can vie for access to the memory. Accordingly, the situations where an arbiter is needed do not arise in Nojima.

Sugita specifically states that their invention "is applicable to dual port memories." Since Nojima does not show a dual port memory, according to Sugita, their invention is not applicable to Nojima. Accordingly, for at least these reasons, there is no motivation to combine the arbitration circuit of Sugita with the memory circuit of Nojima.

For at least these reasons, claim 1 should be allowed.

Claim 7

Claim 7 stands rejected under 35 U.S.C.§ 103(a) as being unpatentable over Nojima in light of Sugita. But this combination of references do not show or suggest each and every element of this claim. For example, claim 7 recites "a programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic functions." These references do not provide this feature.

The pending office action cites the Main Control Decoder Sequencer 60 in Figure 1 of Nojima as showing a programmable logic portion. (See pending office action, page 4, fourth paragraph.) But again, Nojima does not describe this circuit as being programmable, rather it is a fixed logic circuit configured to provide a specific logic function. (See Nojima,

column 3, lines 11-33.) Thus, this circuit is not programmably configurable to implement user-defined combinatorial or registered logic functions as required by the claim.

Claim 7 further recites:

> wherein when the second port is accessing a subset of the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing the subset of the first plurality of memory cells, the arbiter allows the first port to access the second plurality of memory cells. (applicants' claim 7)

The cited references do not provide this feature.

The pending office action cites Sugita, column 2, lines 38-47 and column 7 line 34 through column 8 line 49 as providing this. However, the first of these passages simply states that an arbitration circuit is used. The second describes the connections of the arbiter. The only details on how access is granted is that access rights are granted based on "a predetermined priority." This does not anticipate the arbiter preventing access to a first plurality of memory cells and allowing them to a second plurality of memory cells when a subset of the first plurality of memory cells is being accessed, as is required by the claim.

For at least these reasons, claim 7 should be allowed. Claim 7 should also be allowed for similar reasons as claim 1.

Claim 47

Claim 47 stands rejected under 35 U.S.C.§ 103(a) as being unpatentable over Nojima in light of Sugita. But this combination of references do not show or suggest each and every element of this claim. For example, claim 47 recites "wherein the first plurality of memory cells consists of a number of memory cells and the number is configurable." The cited references do not provide this feature.

The pending office action states that this claim is rejected for the same reasons as claim 7. (See pending office action, page 6, first paragraph.) But as discussed above, the only mention of the arbiter in Sugita is that access is granted based "a predetermined priority." It does

not even mention a first plurality of memory cells, much less that the number of memory cells in the first plurality is configurable.

For at least these reasons claim 47 should be allowed. Claim 47 should also be allowed for similar reasons as claims 1 and 7.

Other claims

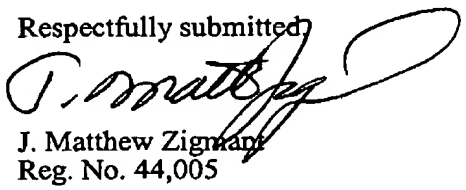
The other claims depend on these claims, and should be allowed for at least the same reasons, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-273-4782.

Respectfully submitted,



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